ATD Tracker Subsystem Development

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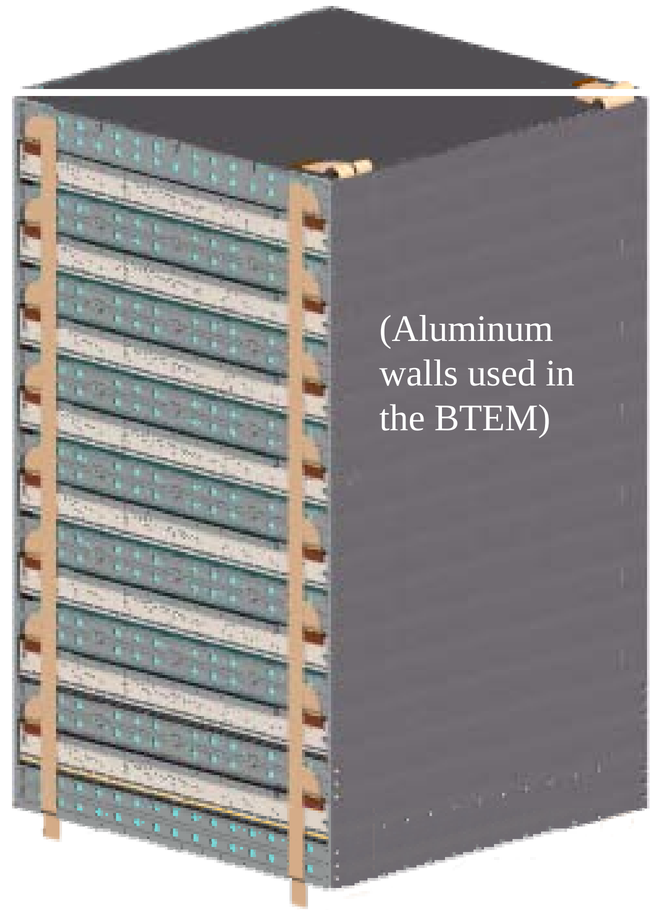
- Overview & Deliverables
- Overview of the BTEM Tracker
- Silicon-Strip Detectors
- Detector Ladder Assembly and Placement
- Readout Electronics
  - Requirements
  - Readout Scheme & Hybrids
  - ASICs
  - Bias circuit & kapton cables
- Tracker Trays
  - Mechanical design
  - Vibration test
  - Assembly
- Tracker Assembly and QC
- Tracker Performance
- Tracker self triggering
- Milestones and Conclusions

Tracker Deliverables for Option 1

- ✓ Make a complete, detailed engineering design of the tracker module.
- ✓ Update the existing Monte Carlo model to finalize our understanding of the instrument performance.
- ✓ Construct a complete Tracker module.
  - Demonstrate low-noise, low-power amplifiers.
  - Demonstrate high-throughput front-end of tracker data acquisition.
  - Demonstrate tracker self triggering.
  - Develop assembly and QC techniques.
- ✓ Integrate the Tracker module with the BTEM Calorimeter, ACD, and DAQ and operate in the SLAC test beams.
- Assess the BTEM performance as a gamma-ray telescope and verify the Monte Carlo simulations (in progress).

Overview of the BTEM Tracker

- One tower with 32 cm × 32 cm of Si.
- 17 “tray” modules (aluminum closeouts).
- 16 *x*,*y* planes
    - 11 with 2.5% X_0 Pb on bottom
    - 3 with 25% X_0 Pb on bottom
    - 2 with no converter
  - Every other tray rotated by 90°, so each Pb foil is followed immediately by an *x*,*y* plane (2 mm gap between *x* and *y*).
- Electronics on the sides of trays
  - Minimize gap between towers.
  - 8 readout modules on each of 4 sides.
- Trays stack and align at their corners.
- The bottom tray has a mounting flange.
- Aluminum walls provide stiffness and thermal pathway to the base.



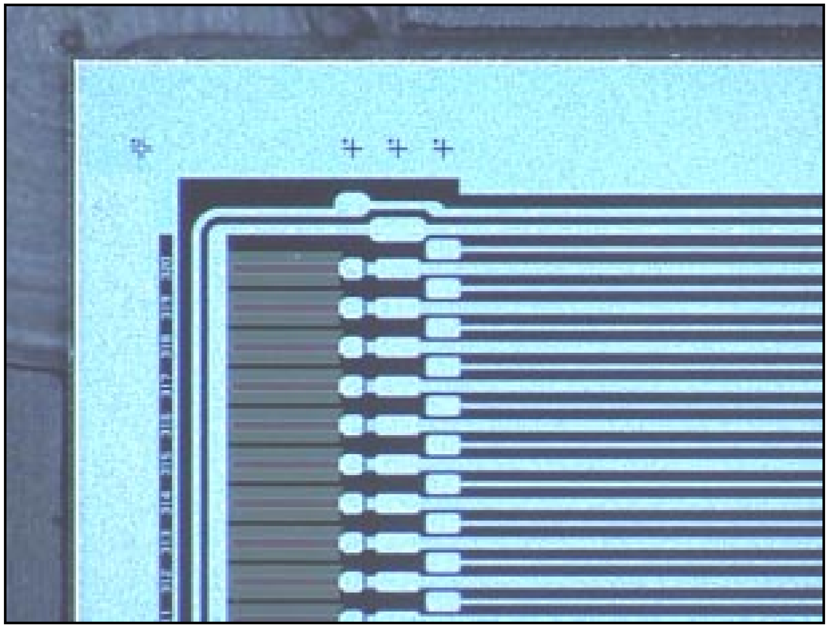
BTEM Tracker Module

Silicon-Strip Detectors

- Description:
  - 400 µm thick, single sided
  - 194 µm strip pitch in BTEM
  - AC coupled with polysilicon bias
- BTEM prototype detectors:
  - 296 detectors from 4” wafers from Hamamatsu Photonics (HPK)
  - 251 from 6” wafers from HPK
  - 5 of the large size from Micron Semiconductor.
- Very high quality! From HPK:
  - Typical leakage: 300 nA/detector
  - Bad strips: about 1 in 5000
- Development of the flight design and qualification of new vendors in progress:
  - 35 9.5-cm square detectors from HPK
  - Prototypes on order from ST (Italy)

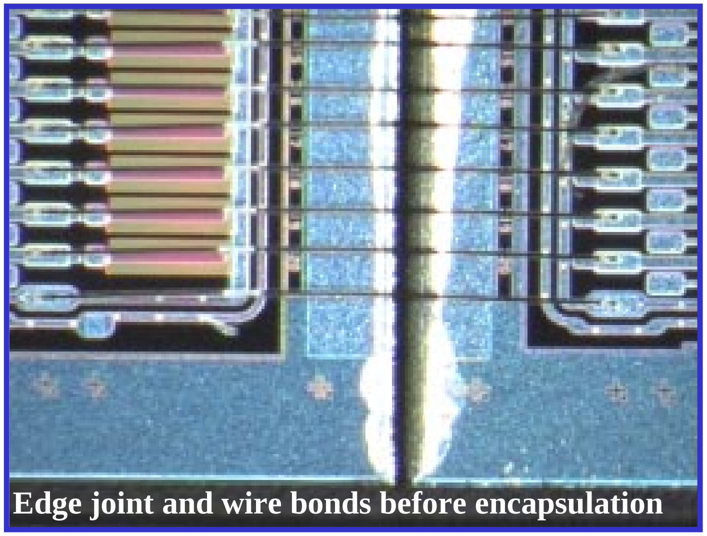
Lessons from the BTEM experience:

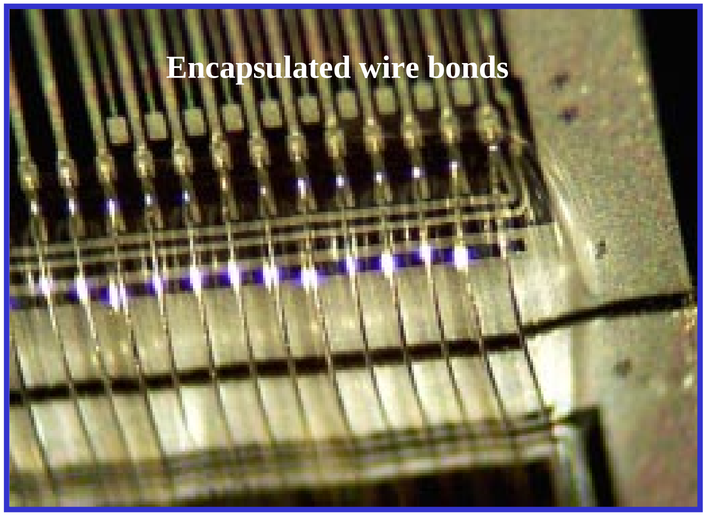
- Bypass strips are not needed, due to low number of bad strips.
- DC pads should be increased in size for ease of testing.
- A second AC pad should be added on each strip, for probing and for a second chance at wire bonding.



Si Detector Ladders

- Detectors were edge bonded at SLAC by hand, using a simple alignment jig.
  - Some problems with vertical steps on the larger detectors, and better control needed of the glue joint.
  - Alignment in the plane: ~30 µm typ.
  - A more sophisticate gluing jig is under development to improve QC and alignment.
- Wire bonding is straightforward.
  - Only 0.06% of wire bonds needed repair.
  - No evidence of strip damage from the wire bonder.
- Wire bonds were encapsulated with a hard curing epoxy.
  - Epoxy was sprayed onto the bonds through a slit.
  - Good results were obtained, but the procedure needs more development for efficiency and control.
- Only 18 of 41,600 BTEM ladder strips were partially defective in the end!


Edge joint and wire bonds before encapsulation

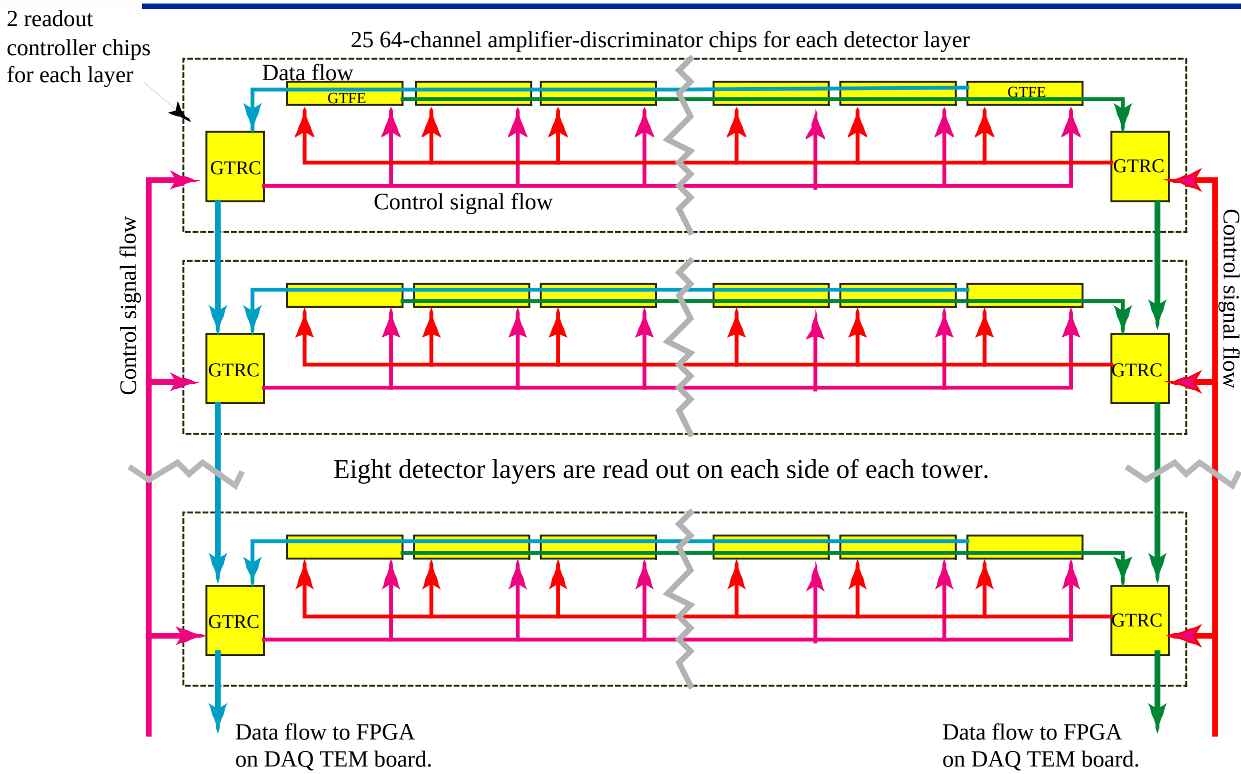

Encapsulated wire bonds

Tracker Readout Electronics Requirements

- Noise occupancy $<5\times10^{-5}$ with an efficiency of >99% for minimum ionizing particles (within fiducial region).
- Low power (<240 μW/ch).
- Self triggering.
- Sustain 10 kHz trigger rate with <10% dead time.
- Radiation hard to >10 kRad.
- Single-event latchup resistant to > 20 MeV-cm^2/g LET.
- Configuration registers SEU resistant to >3 pC charge deposition.
- Redundant readout scheme to minimize the possibility of catastrophic single-point failures.
- Compact, to minimize inter-module dead space.

(Note that the detailed numbers here are TBR.)

Tracker Readout Concept



GLAST tracker front-end readout scheme, as implemented in the BTEM.

Built around two custom ASICs: GTFE64 and GTRC.

8 layers read out on each of the 4 sides of the BTEM tower, each with 1600 channels.

- Two redundant paths for control signals, trigger information, and data output.
- Any single chip or cable can go bad without affecting readout of the remaining chips.
- Zero-suppressed data from the entire tower flows out in one, or two, serial data streams.
- Complete zero suppression and formatting takes place in the digital GTRC chips.

Front-End Readout Chip (GTFE64)

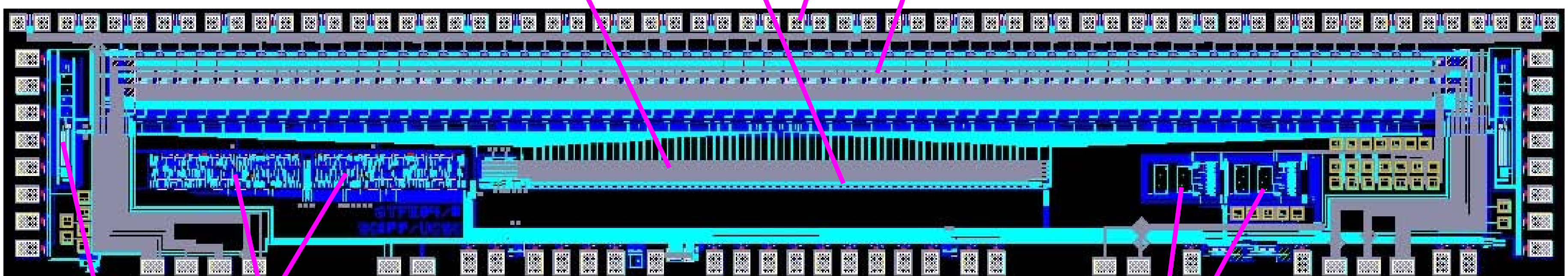
- Several thousand were made in the HP 0.8 μm process for the BTEM and gave very good performance. This process no longer exists.
- Prototypes of just the amplifiers and discriminators fabricated in the HP 0.5 μm process are under test at UCSC and, preliminarily, appear to be working well.

Input pads for 194 μm pitch detectors

Two redundant readout registers

64 amplifier-discriminator channels, proven in beam test

Buffering for 8 events



Dual redundant serial command decoders

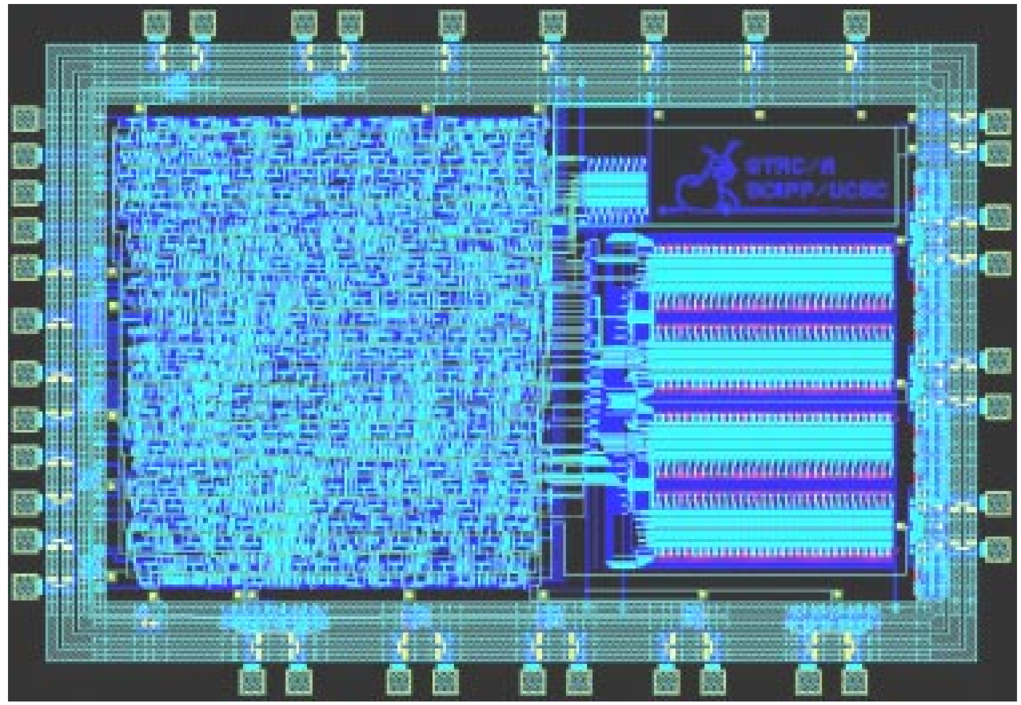
Front-end readout chip, as used in the BTEM.

Low Voltage Differential Signaling

DACs for threshold and calibration levels

Readout Controller Chip (GTRC)

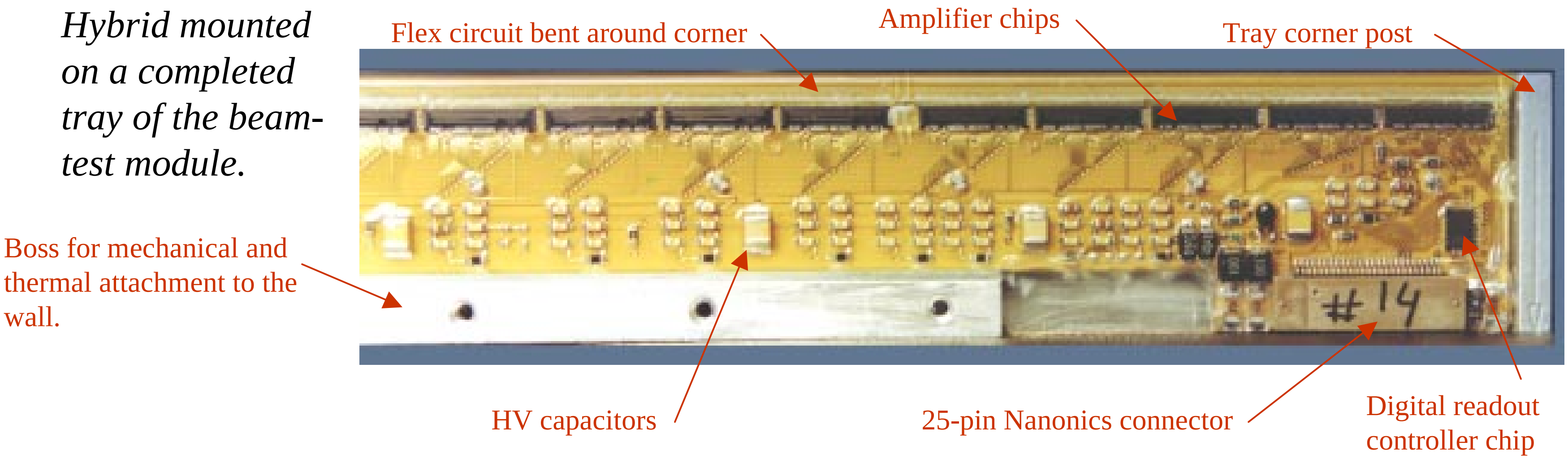
- Full custom CMOS IC, fabricated in the HP 0.8μm process for the beam-test tower.
- Logic design and layout uses DoD standard cells.
- Functions:
  - Zero suppression and formatting of the data.
  - Command and clock interface to the front-end chips.
  - Sequencing and buffering of the readout.
  - Time-over-threshold of the Fast-OR trigger output.
  - Communication via low-voltage differential signaling (LVDS).
- Functioned reliably in the 1999 beam test at SLAC.
- The flight version will be done in the HP 0.5 μm process (TBR).



Cadence layout of the GLAST Tracker Readout Controller chip (GTRC). The left half is logic made from standard cells, while the right half is memory for buffering.

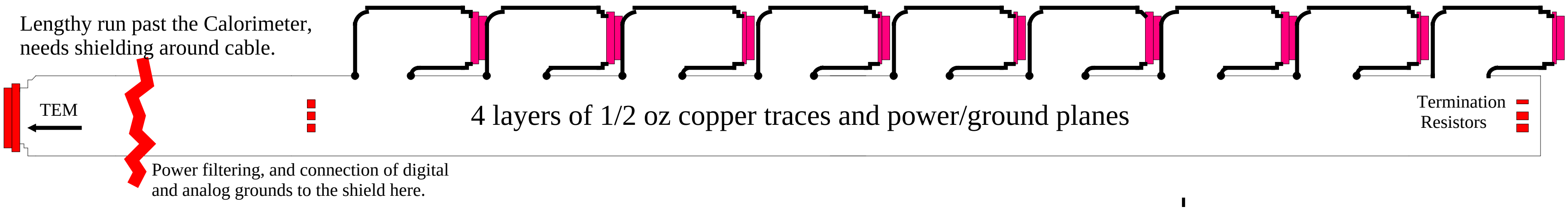
Hybrid PC Board

Hybrid mounted on a completed tray of the beam-test module.

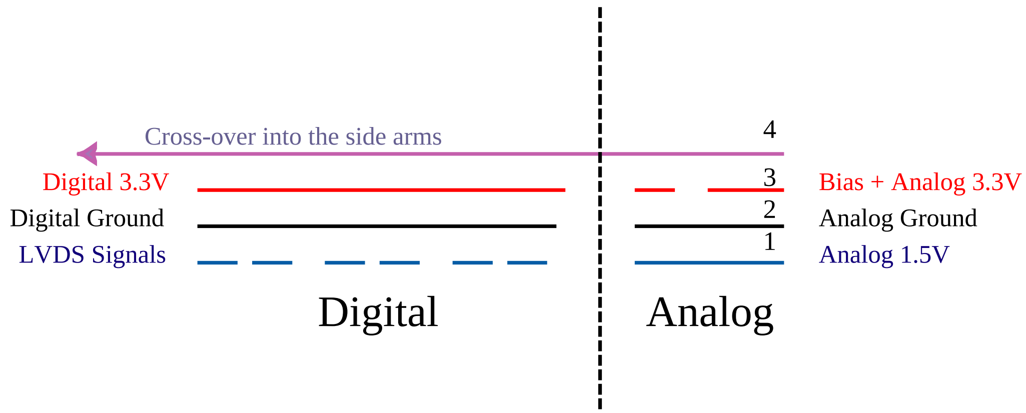


- 25 64-channel amplifier chips and 2 digital readout chips on each board (1600 ch.)
- 8-layer standard FR4 PC board with minimum 4-mil traces and spaces.
- Gold body for wire bonding. Conformal coated after assembly.
- Lots of filtering and decoupling for bias, power supplies, etc.
- Careful attention to shielding between analog and digital and to maintaining clean current returns for the detector signals.
- Temperature monitoring built in.
- ***Excellent performance in the 1999 beam test. No evidence of noise isolation or grounding problems.***

Tracker Readout Cables



- Custom 4-layer flex circuits
- Standard processes, with Kapton and 1/2 oz copper.
- Connectors and other components are surface-mount soldered.

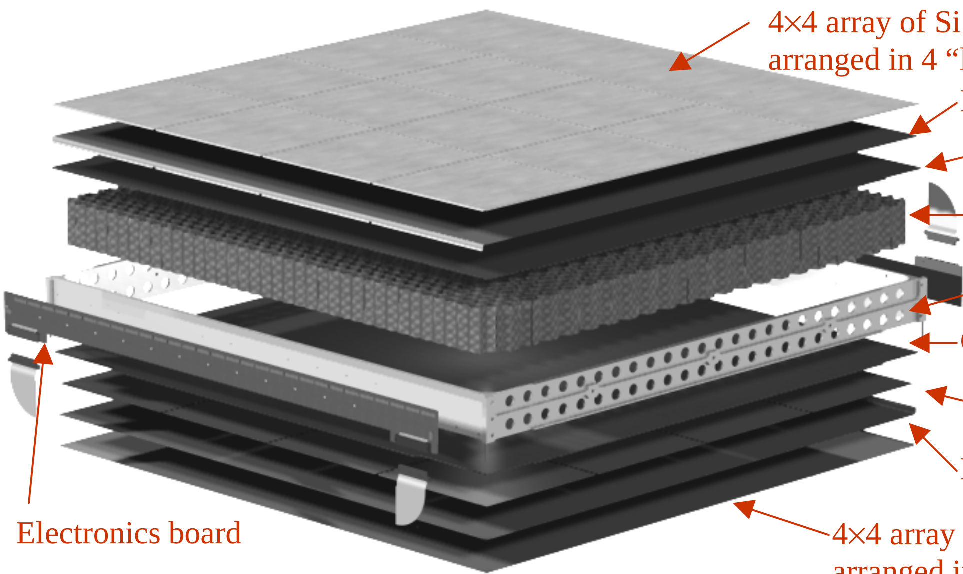


4-layer cable cross section, showing a schematic representation of the arrangement of conductors.

- Good electrical and mechanical performance was achieved in the BTEM with these cables.
- The flight design will need to be longer, to pass by the calorimeter. A connector-splice in the middle may be required. No flight qualification work has yet been done.

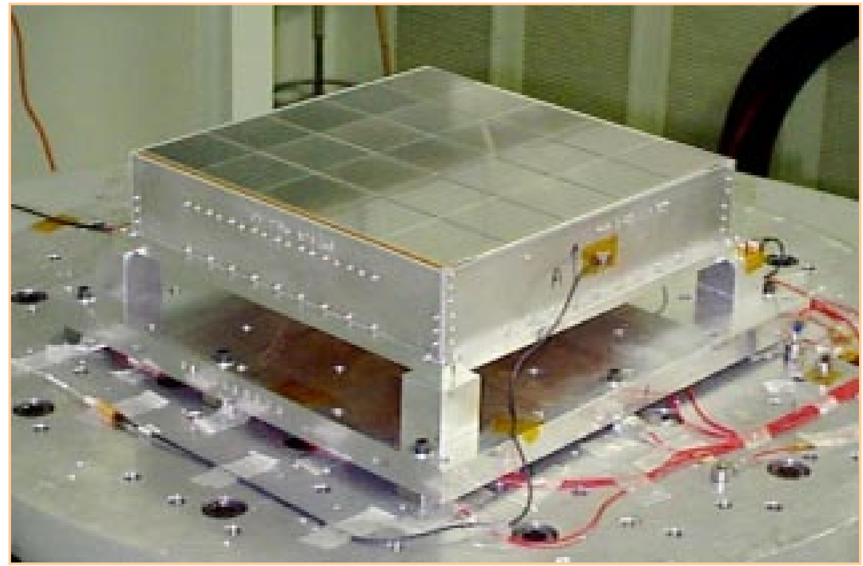
Tracker Module Mechanical Design

- The tray must be very stiff to avoid collisions (f_0>500 Hz).
- All prototypes to date have been made with machined aluminum closeouts—high multiple scattering and poor thermal matching.
- A development effort is in progress at Hytec Inc. (Los Alamos, NM) to make tray structures entirely from carbon fiber.
- Hytec is also developing the carbon-fiber walls, hex-cell cores, and face sheets.



Tray Shake Test

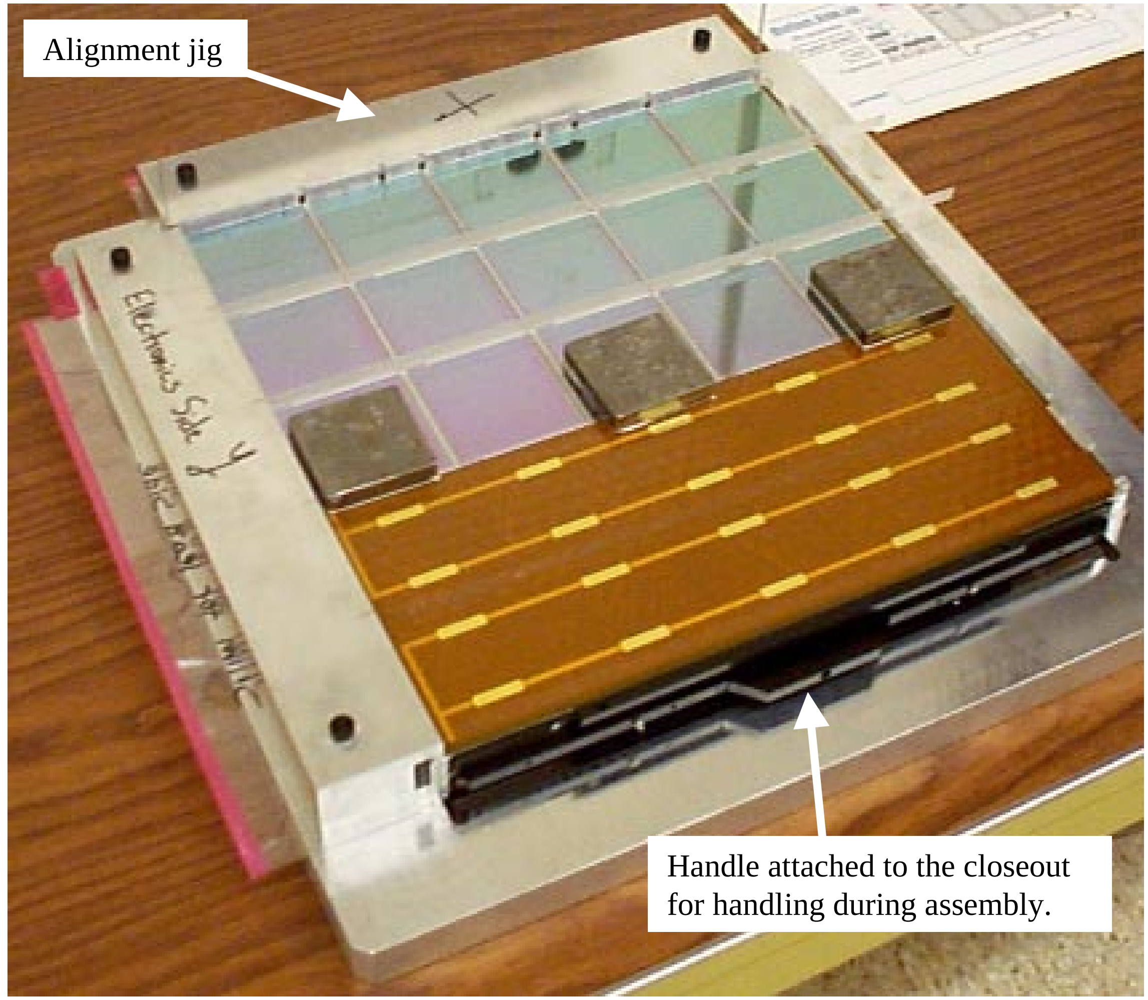
- Two trays, one with live detectors and electronics, were vibration tested at GSFC.
- Random-vibration testing to full GEVS qualification levels did not produce any detectable damage (including no broken wire bonds) and did not affect detector leakage current.
- The first resonance was well above 500 Hz, demonstrating sufficient stiffness to avoid tray-tray collisions during launch.
- The data are presently being used to verify models in use for the development of a carbon-fiber tray design.



Vibration test setup at GSFC, for a tray with a full compliment of live detectors on top. The detectors are wire bonded to readout electronics.

Ladder Placement on Trays

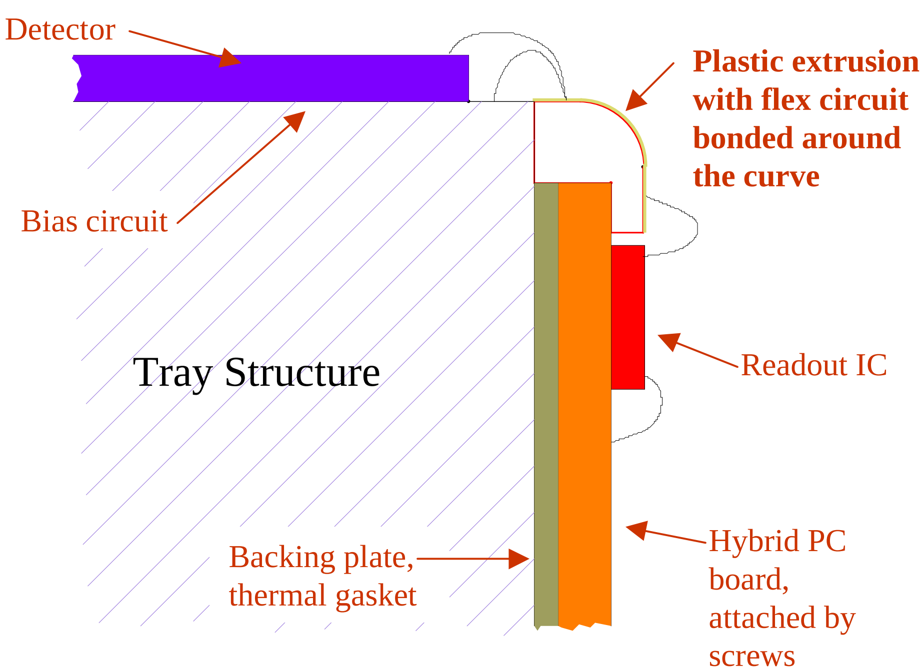
- Ladders were aligned with respect to the holes in the corner posts, by pressing against a straight edge.
- Shims set the spacing between ladders.
- Space-qual. silver-loaded epoxy was used to bond detectors to the bias circuit.
- 50 µm thick tape set the adhesive bond thickness.
- *The resulting precision was marginal and subject to error buildup. A more sophisticated procedure is being designed.*
- *Lots of issues with adhesives and thermal stress are currently under investigation.*

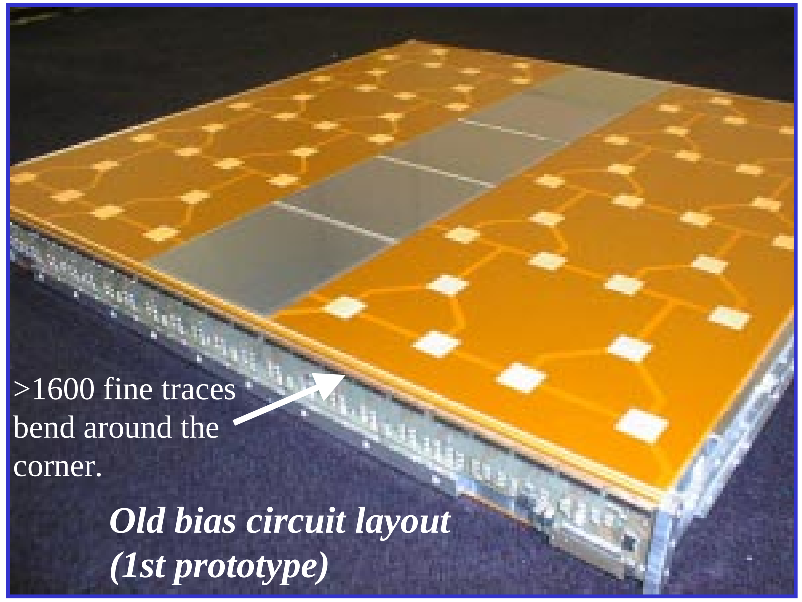


Electrical Mounting

BTEM scheme: 2-layer Kapton flex circuit

- Top layer: pads for conductive adhesive, to carry the bias current to the detectors.
- Bottom layer: hatched ground plane, to isolate the detector bias from tray structure.
- Tongue with >1600 narrow traces carry signals and bias around the tray corner.
- **Difficult to mount and align electronics.**





Old bias circuit layout (1st prototype)

New concept under development (illustrated at left):

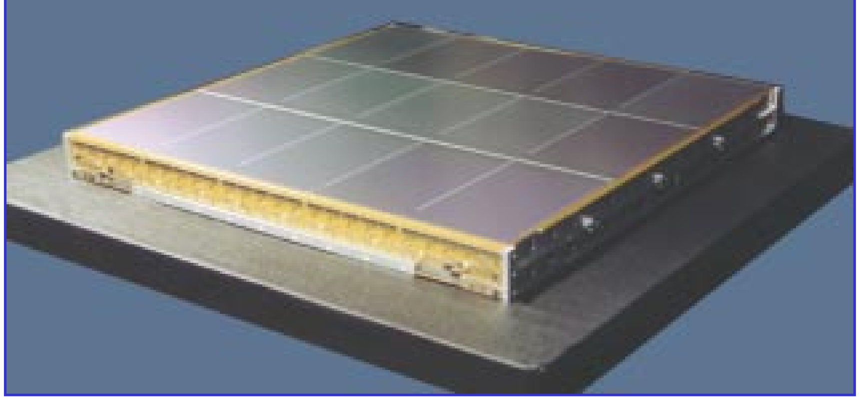
- The flex circuit for wrapping around the corner is separate from the bias circuit and is part of the hybrid assembly.
- It has 1 trace for each detector strip, plus bias and ground connections for each ladder.

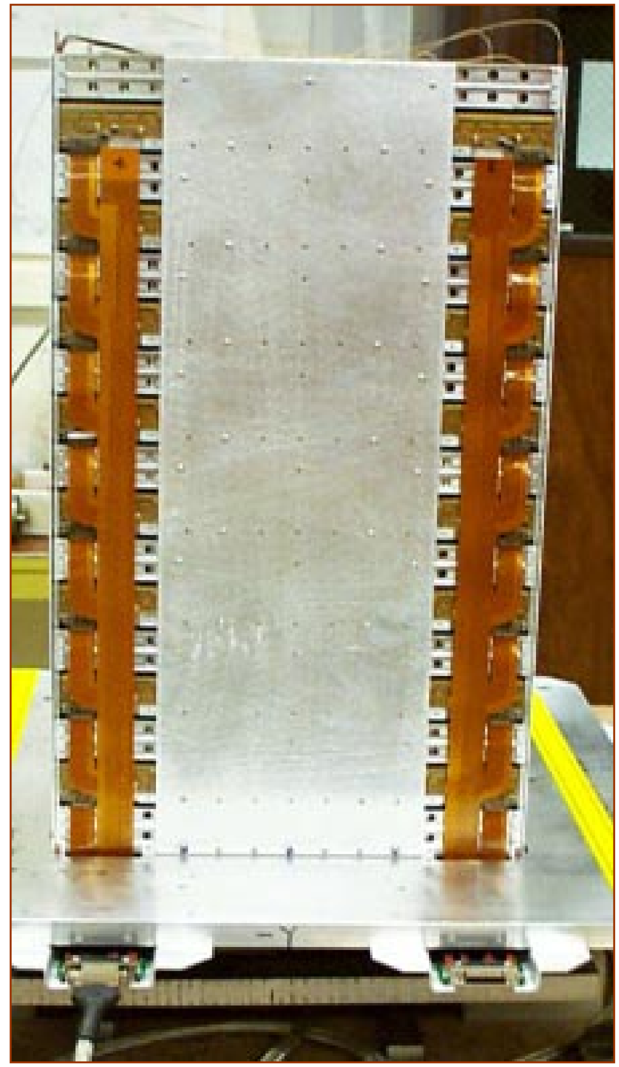
BTEM Tracker Assembly

Assembly of the completed trays into a tower went very smoothly and gave good alignment (verified by CMM).

- 17 trays, 16 *x,y* planes
- 51,200 amplifier-discriminator channels, with 41,600 connected to detector strips.
- 130 32-cm detector ladders (out of 160 needed for the complete device), for 2.6 m^2 of silicon.
- 11 *x,y* planes with 3.5% Pb foils
- 3 *x,y* planes with 25% Pb foils

Single completed tray, detectors top & bottom





The completed beam-test tracker, with 2 side panels removed.

BTEM Tracker QC

Some of the Testing Done:

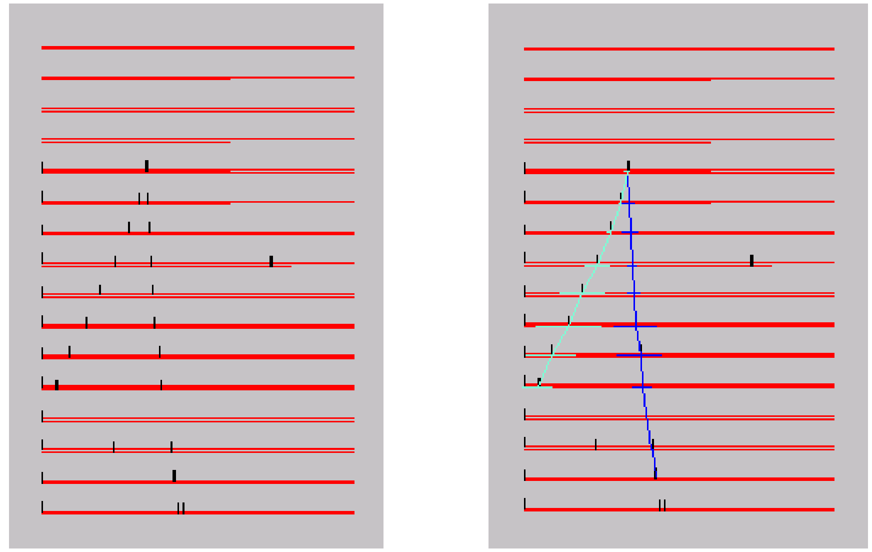
- Detectors tested by manufacturer (IV and coupling cap) and visually scanned by us.
- IV curves taken again after edge bonding, wire bonding, and before mounting on the tray.
- Capacitance measured on an automatic probe station for each strip after wire bonding to detect broken caps, broken metal, missing wire bonds, and shorts. *Only 18 bad strips found and isolated by removing wire bonds.*
- ICs thoroughly tested on the wafer by an automatic probe station.
- Hybrids tested and burned in before mounting on trays.

- *The result is only a handful of dead or noisy channels, plus one noisy ladder* (as yet unknown reason).

Setup used to test 8 trays at a time with cosmic-rays and the actual DAQ. The trays are still in protective plastic enclosures and have aluminum handles attached to the sides.

Beam-Test Tracker Performance

Analysis of the PSF is in progress, but the tracker reconstruction software is already highly developed and working well.



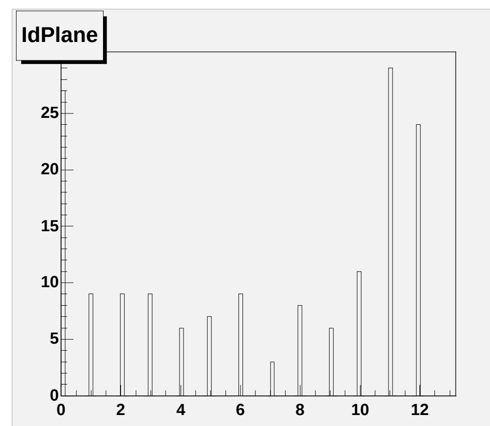
A single photon conversion from beam-test data, before and after track finding and fitting with a Kalman-Filter algorithm.

Data were taken for

- cosmic rays
- positrons at various energies
- tagged photons
- mixture of hadrons and positrons

The tracker ran reliably for 2 months with no changed needed in threshold settings or masks (no channels were masked) and no change in leakage.

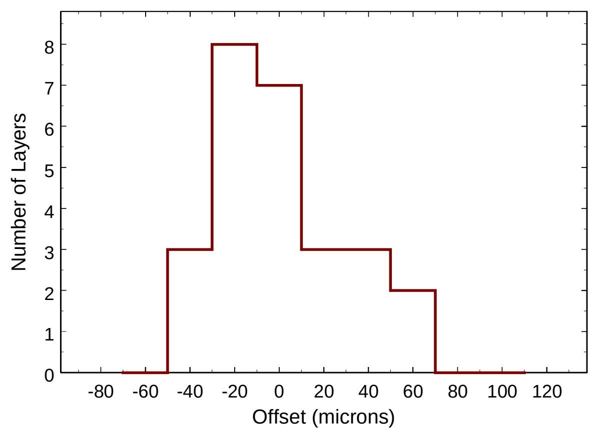
Distribution of photon-conversions per tracker plane.



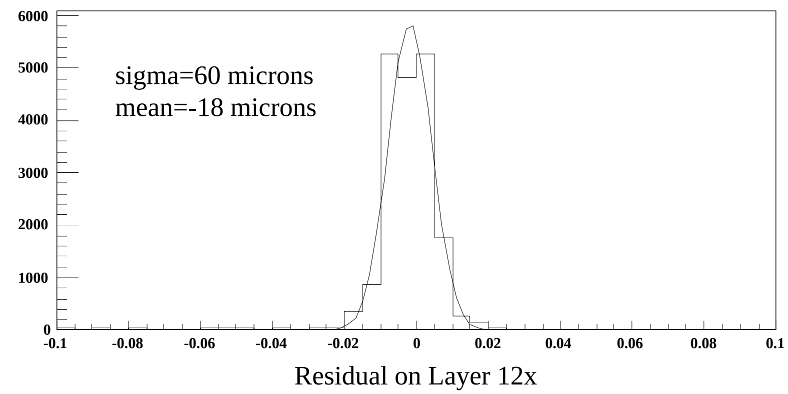
The self trigger worked well, but most data were taken with a beam trigger.

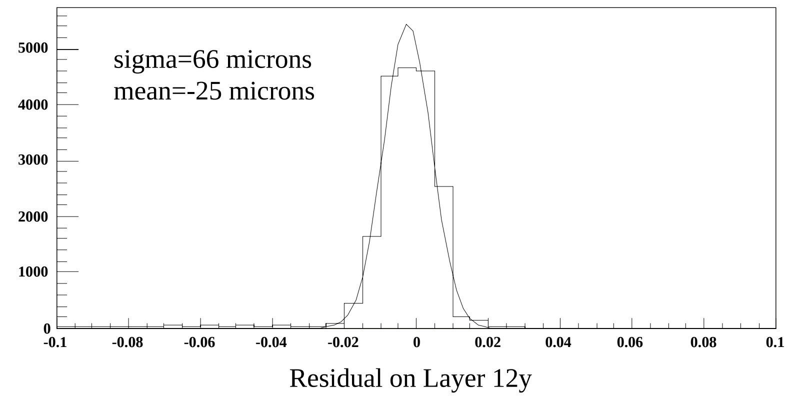
Tracker Tower Alignment

- Tray-to-tray alignment has been looked at in cosmic-ray and positron data and appears to be within our goal of 50 micron rms.
- More analysis is in progress with a position scan of hadron data, to get uniform coverage and enough sensitivity to study rotations.



Offsets from 26 of the 32 layers, as obtained from 20-GeV positrons.

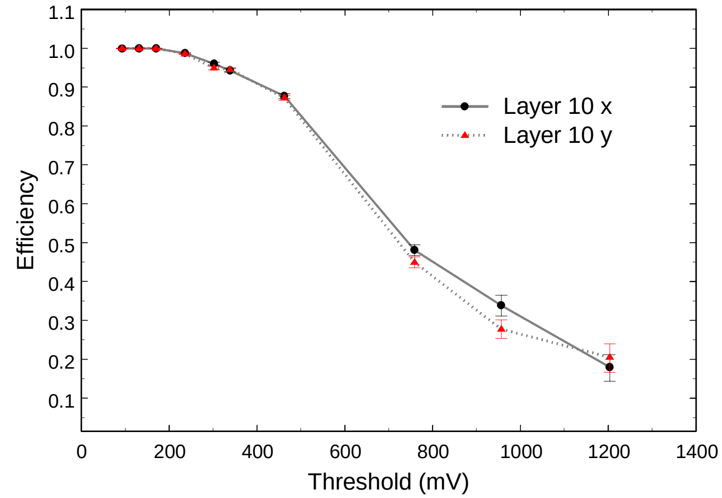




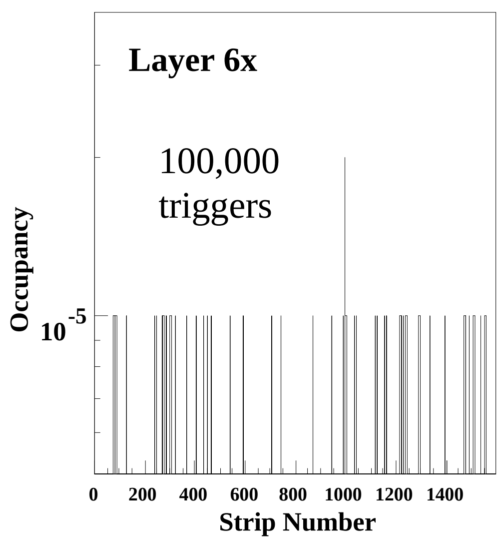
Residual distributions on Layer 12, from fitting 20-GeV positron tracks to straight lines in layers above and below. The width is as expected for 194 μm pitch.

Tracker Noise and Efficiency

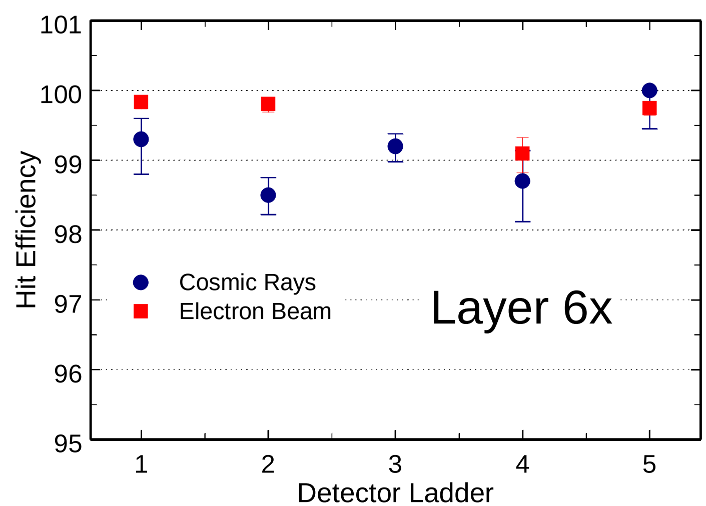
- Noise occupancy was obtained by inducing triggers, followed by readout, at random times.
- Hit efficiency was measured using single electron tracks and cosmic muons.
- ***The requirements were met: 99% efficiency with <<10^{-4} noise occupancy.***
- However, this was with no live trigger during the readout. We are now measuring occupancy during digital activity.



Hit efficiency versus threshold for 5 GeV positrons.



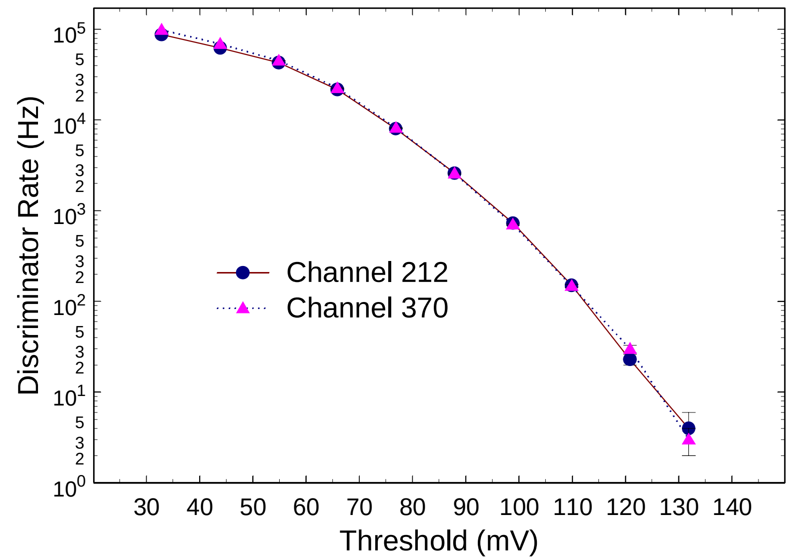
Noise occupancy and hit efficiency for Layer 6x, using in both cases a threshold of 170 mV. No channels were masked.

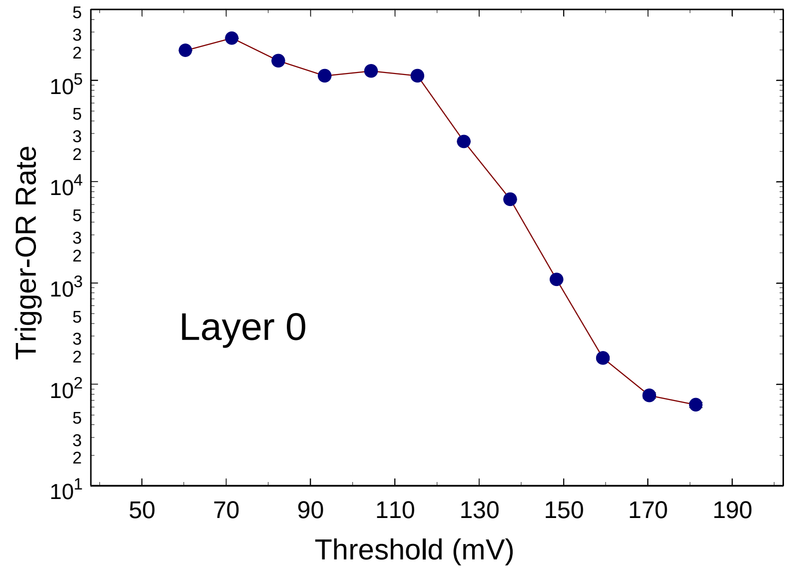


GLAST

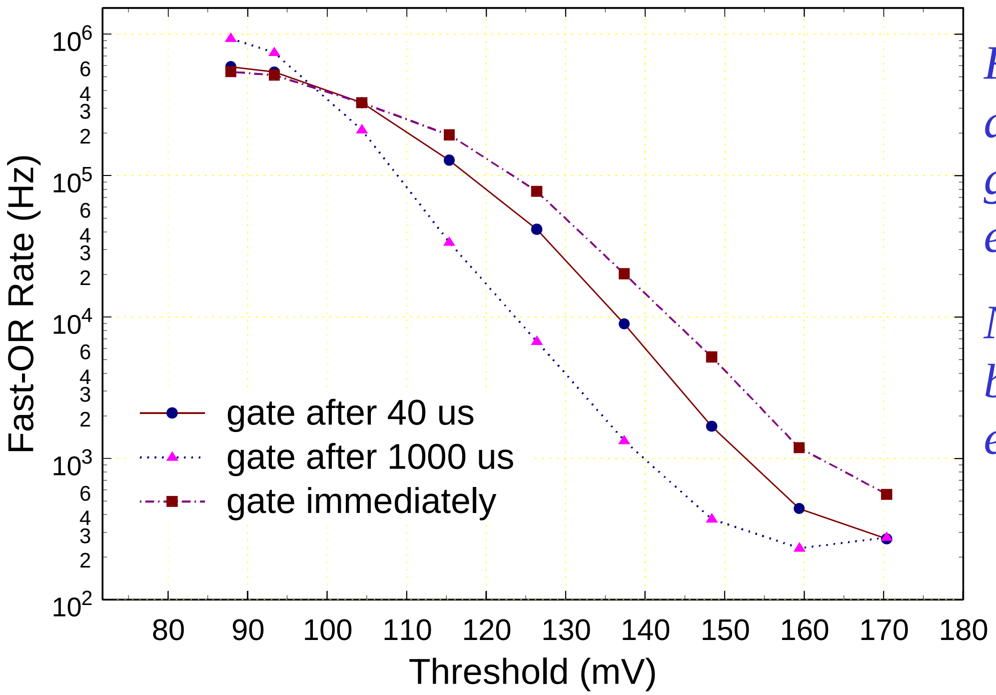
Tracker Self Triggering

- The self-triggering capability of the tracker was demonstrated during the beam test.
- The noise trigger rate was negligible and, in fact, consistent with being mostly from cosmic rays.
- Since the end of the beam test we have been making measurements of the Fast-OR signals (trigger inputs) from individual layers, both with and without concurrent digital readout activity.
- On the right are measurements of the rates from 2 individual channels and the rate from the OR of 1596 channels (4 noisier channels being masked). This is with no concurrent digital activity.
- At the nominal 170 mV threshold setting the noise rate is negligible.





Tracker Trigger During Readout



Fast-OR rate in layer 0 accumulated in a 500 μs gate following a previous external trigger.

Note that the readout begins 30 μs after the external trigger occurs.

The beam test did not demonstrate adequately the trigger noise performance even in the self-triggering run, because of the large dead time imposed by the calorimeter. In nearly every case the tracker readout was finished before the trigger became live again. Therefore, we made the measurements above in the lab, in which we monitored the Fast-OR rate from a layer during the time that a readout is occurring. At the operating threshold (170 mV), the only significant additional noise occurs immediately after the readout clock turns on. ***After that transient has passed, we see no problem from the digital activity.***

Milestones and Conclusions

All of the proposed ATD milestones associated fabrication of the prototype tower have been met, although data analysis from the beam test is still in progress. Test beam operation of the BTEM tracker was an unqualified success.

Proposed	Item	MILESTONES	Actual
6/1/98	Start Program.		7/1/98
7/1/98	Prototype FEE ASIC's tested.	Validation of ASIC design.	8/1/98
7/1/98	Silicon Detectors tested.	Validation of the SSD design.	8/1/98
9/1/98	Test Full length ladder plus electronics	FE elec. design validated.	9/1/98
10/15/98	Prototype tray assembly complete; tray design review.	Tray design and fabrication methods validated.	1/15/99
11/1/98	First production tray assembled	Tray production validated	9/2/99
3/15/99	Last tray complete. Begin prototype tracker assembly.	Validation of the tray assembly QC procedures	10/25/99
5/1/99	Review of tower EMI suppression.		
5/15/99	Prototype Tracker assembly complete		11/15/99
7/15/99	Cosmic Ray test of prototype tracker complete		11/26/99
8/15/99	GLAST tower prototype assembly complete	Validation of the integrated mechanical design and the mechanical/electrical/thermal interfaces	12/1/99
9/1/99	GLAST Tower Prototype Beam Test begins		12/1/99
12/31/99	GLAST Tower Prototype Beam Test complete	Validation of BTEM from beam-test results, compared with MC model.	1/31/00 (anal. in progress)

Milestones and Conclusions

Good progress was also made on taking the tracker design beyond the BTEM.

- Amplifier-discriminator ASICs in the HP 0.5μm process were prototyped & tested.
- The silicon-strip detector design was completed and prototyped.
- Work is in progress on advanced mechanical/thermal designs and precision assembly jigs, but is not yet ready for formal review.

Propose Date	Item	Milestone	Actual Date
6/1/98	Start Program		7/1/98
7/15/98	Silicon Detectors: select redundancy scheme.	Final silicon-strip detector design completed.	8/1/98
12/1/98	Silicon detectors from 6" wafers delivered.		1/15/99
2/1/99	Design Review on precision assembly.	Validation of the production alignment methods.	not yet reviewed
2/1/99	Design Review on advanced tower design.	Thermal/structural design completed.	not yet reviewed
9/15/99	Fabrication of front-end electronics ASICs in new process begins.		9/1/99
12/1/99	Optimized silicon detectors from 6" wafers received.	Validation of the final detector design.	8/1/99