Data Acquisition System

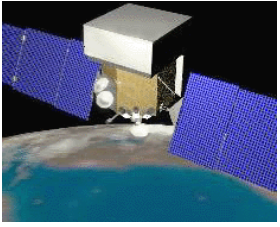## Roger Williamson

Collaboration Meeting

GSFC

### March 20, 2000

GLAST
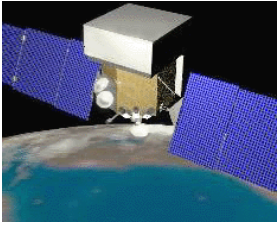
ATD Program

- ◆ Baseline Requirements and Design Evolution

- ◆ Current Requirements and Baseline

- ◆ ATD Results
  - – Performance
    - Level 1 Trigger
    - Read Out
    - Level 2 Trigger
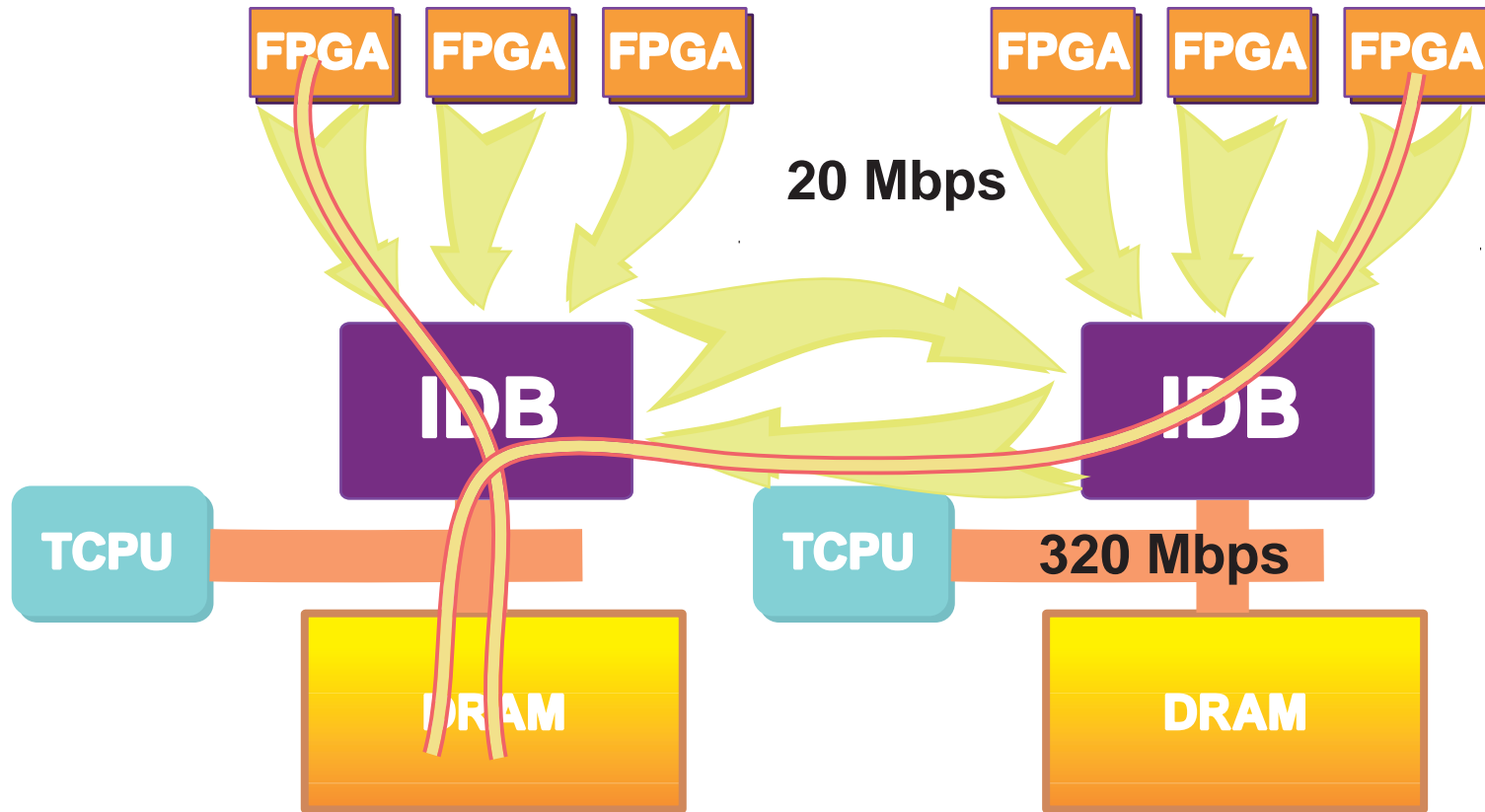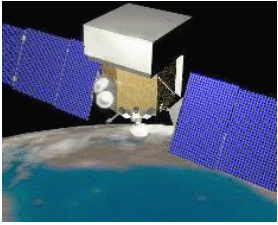 - – Power

GLAST

ATD Project Requirements

- Level 1 Trigger
  - Three-in-a-Row
  - Global Trigger with Veto Capability
- Read Out Detectors
- Downlink Data Rate Constrained
- Power Constrained
- Beam Test Support for Prototype Tower

GLAST
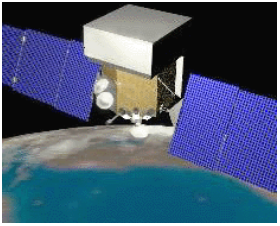
Data Push Functional Diagram
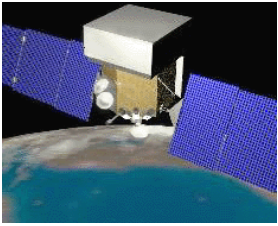

20 Mbps

320 Mbps

GLAST

Data Flow

- ◆ Level 1 Trigger initiates data capture to memory in hardware
  - – 20 usec dead time (max)
  - – Parallel serial read outs for all detectors
  - – Serial to parallel conversion in FPGA
  - – 32 bit wide FIFO buffer holds multiple events
  - – FPGA controls serial transfer over multiple links to DRAM
- ◆ Level 2 Trigger
  - – Not time critical because of large memory buffer space
  - – Local CPU at each tower filters events prior to Level 3 to reduce intertower bandwidth requirement

GLAST

Triggers

GLAST